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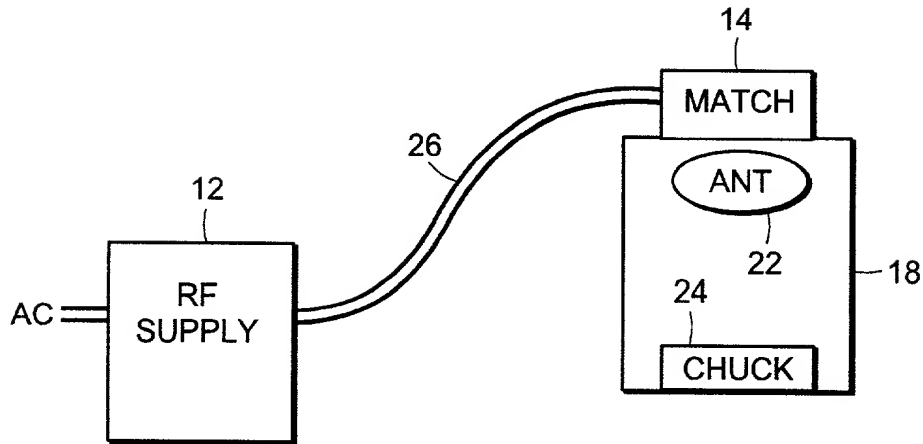


FIG. 1A
PRIOR ART

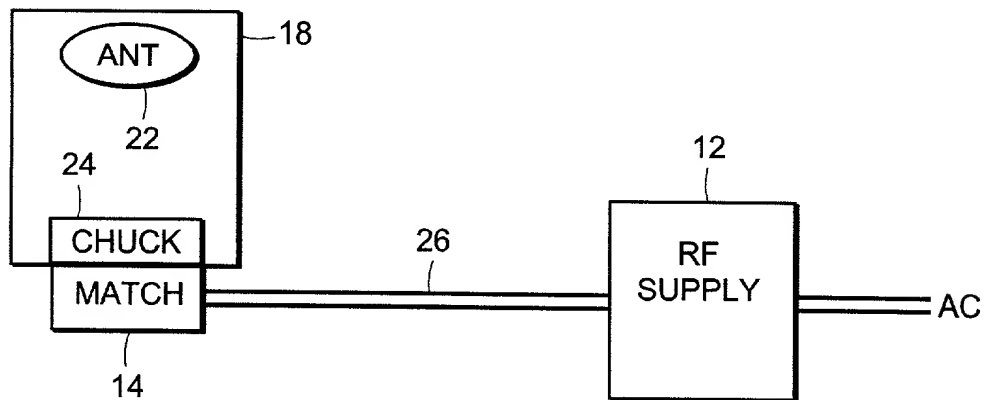


FIG. 1B
PRIOR ART

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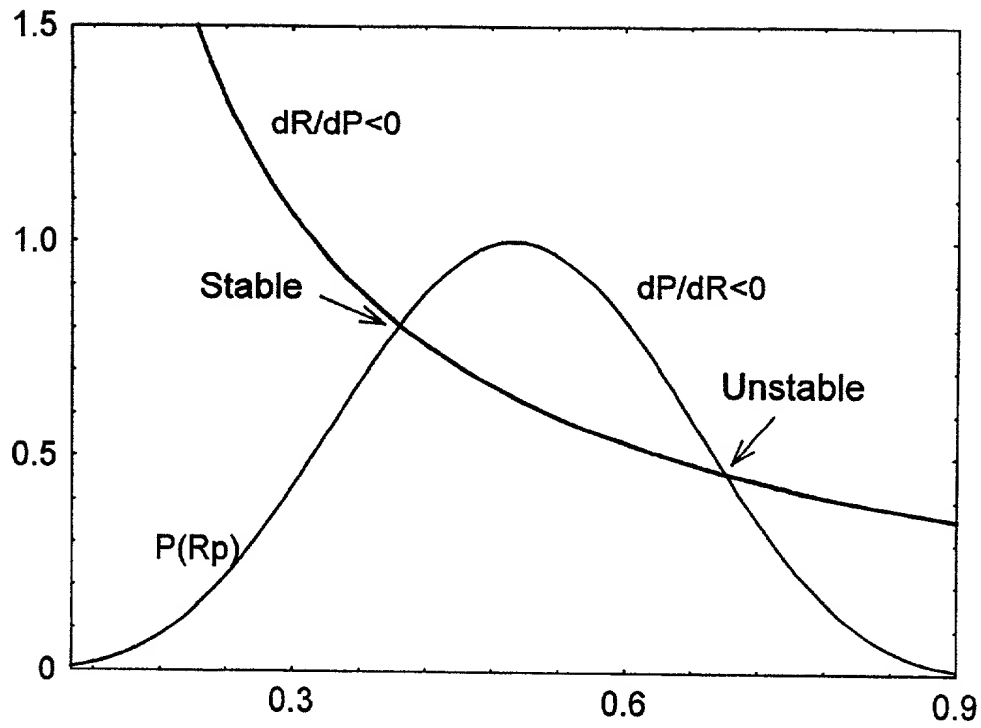


FIG. 2

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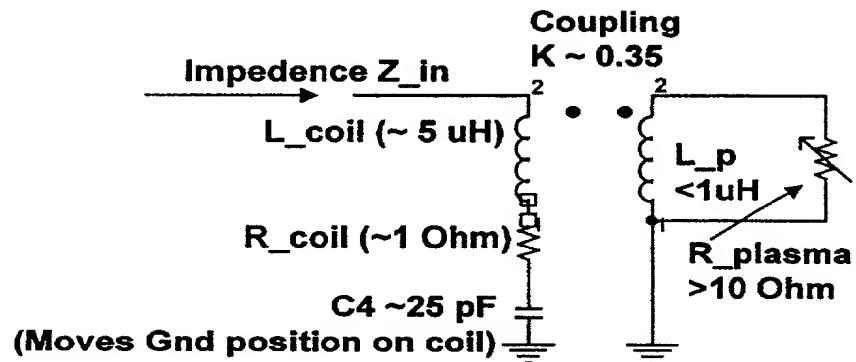


FIG. 3A

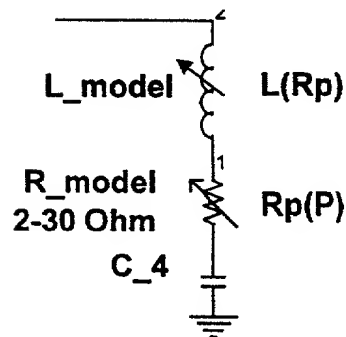


FIG. 3B

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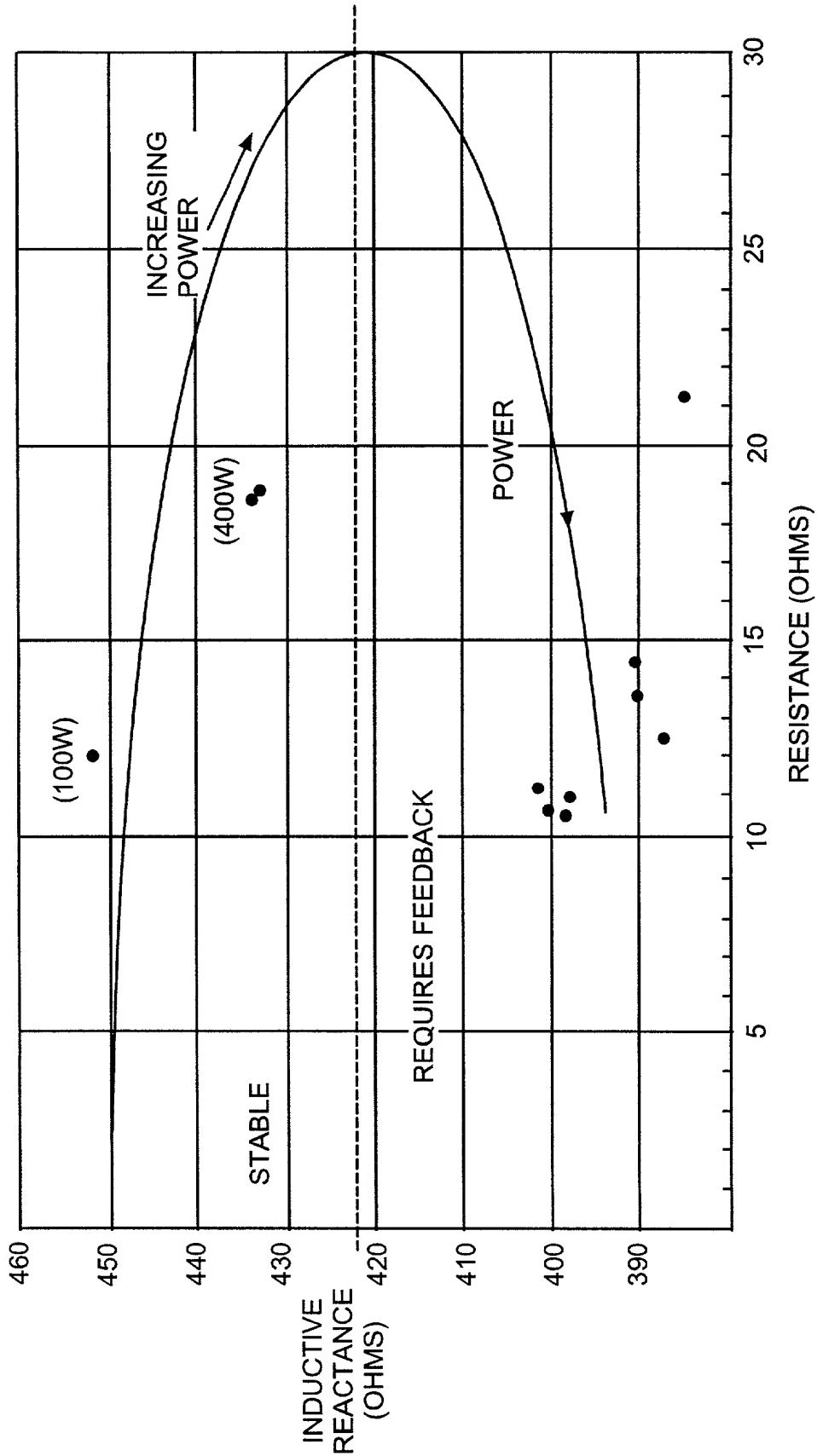


FIG. 4

2026000-12096000

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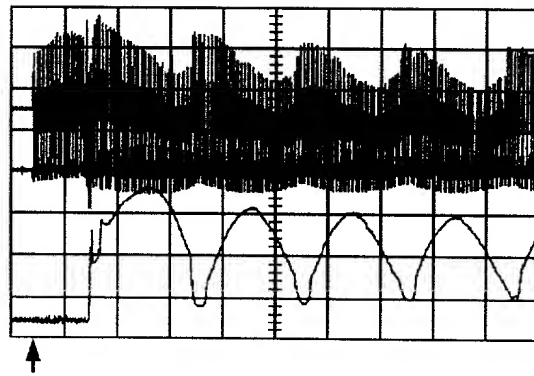


FIG. 5

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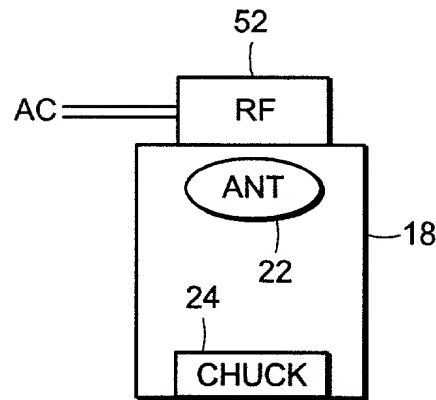


FIG. 6A

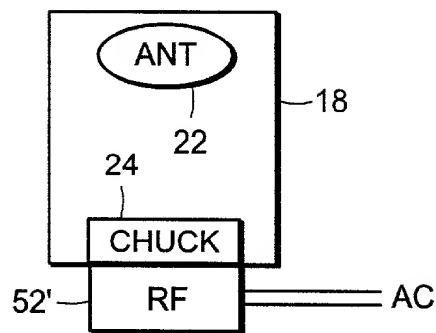


FIG. 6B

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100

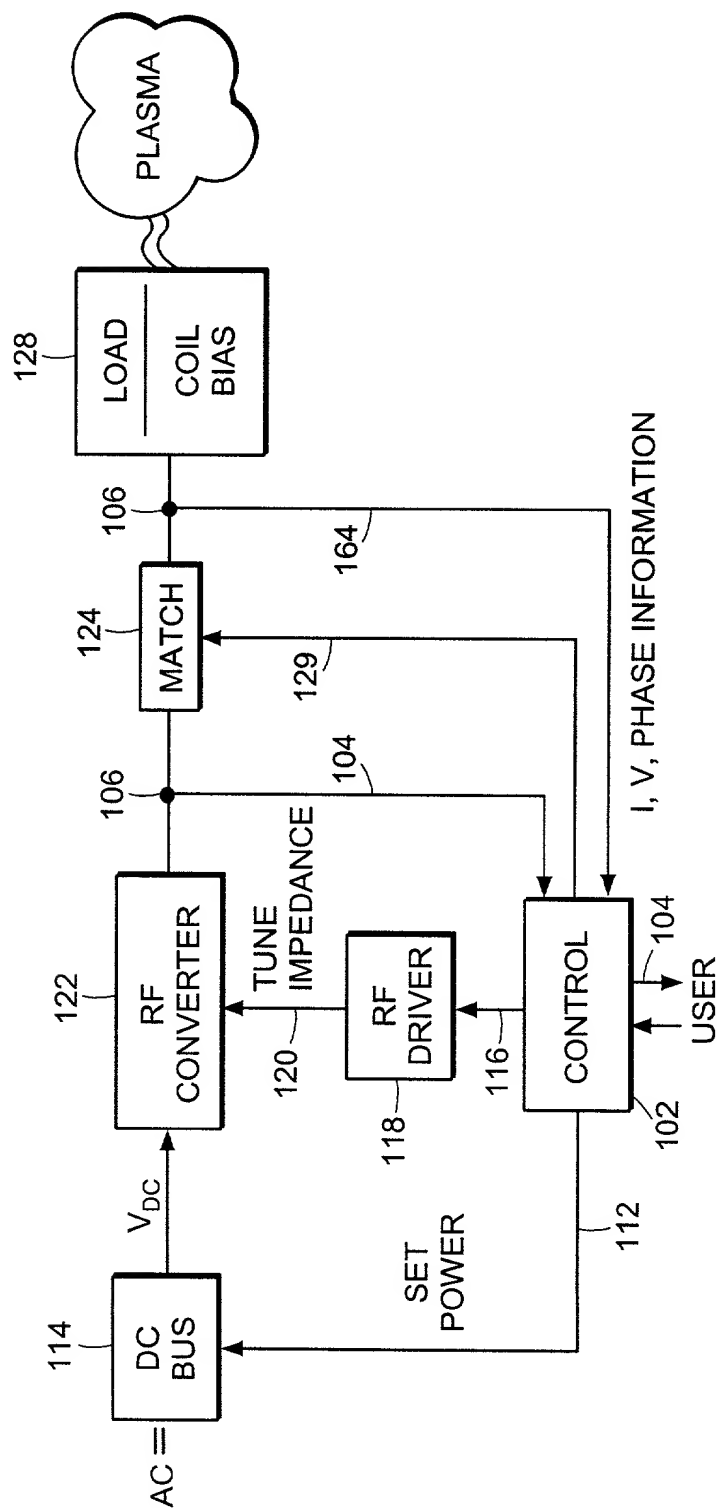


FIG. 7

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150

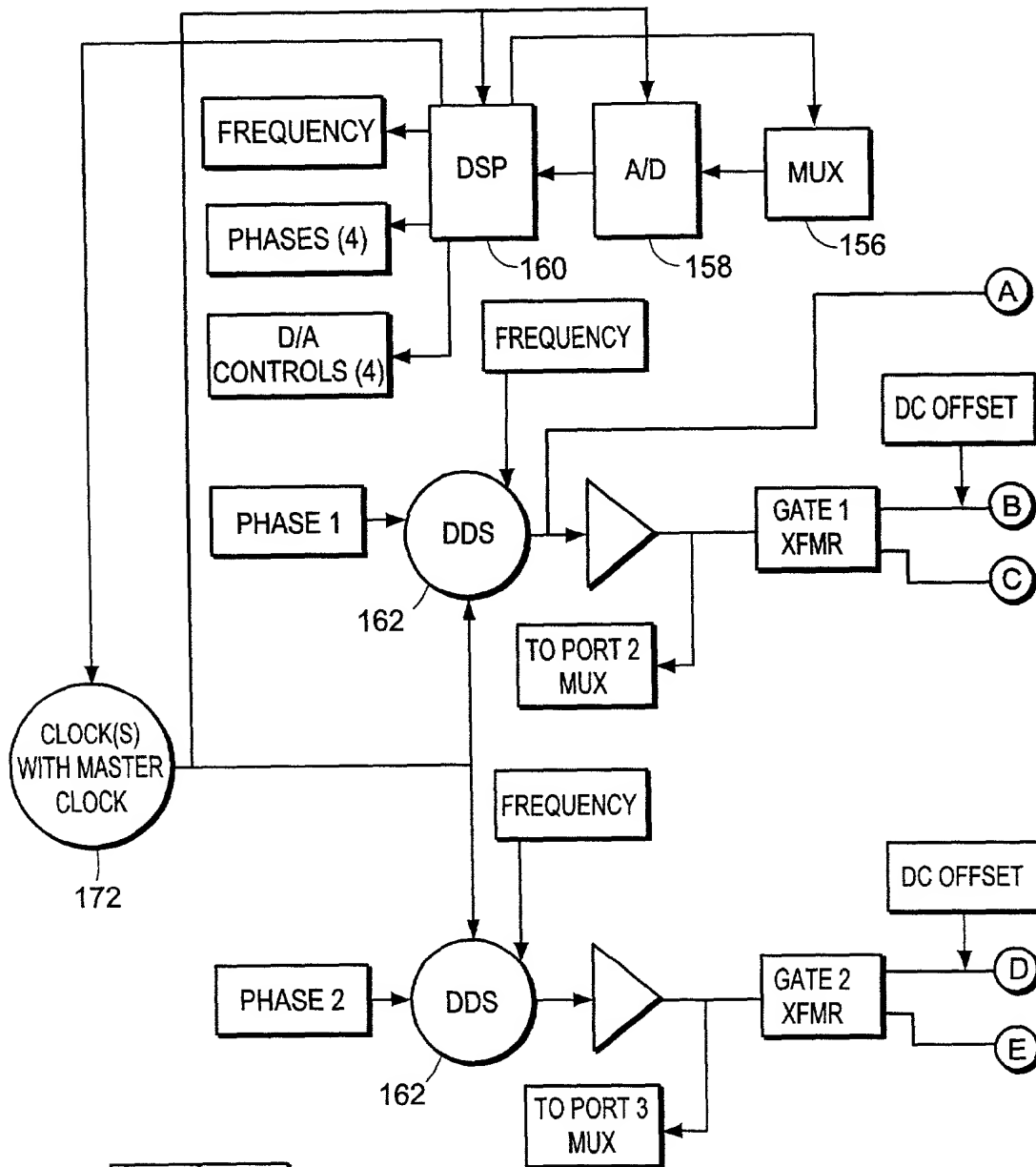


FIG. 8A
 FIG. 8B

FIG. 8

FIG. 8A

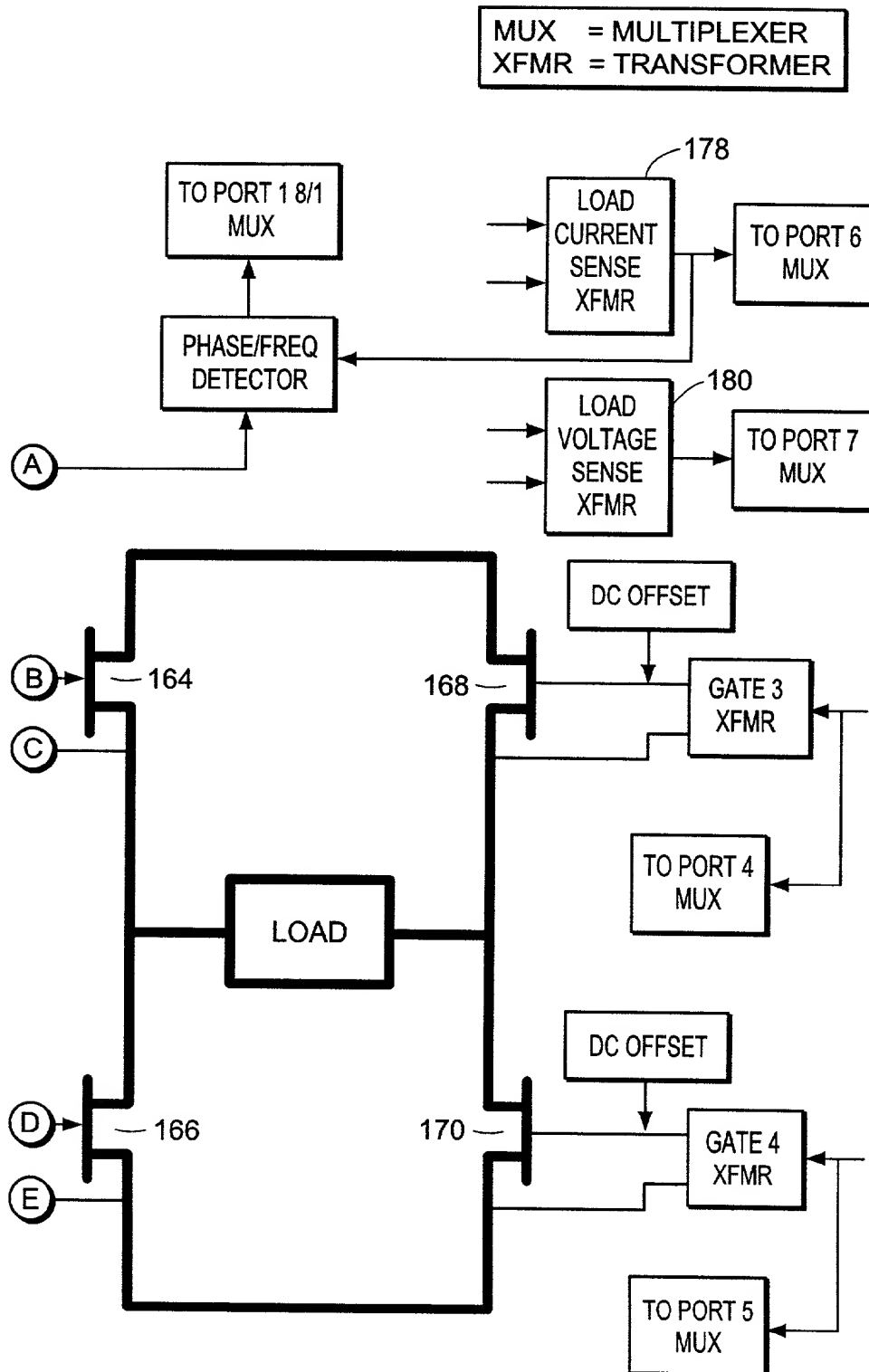


FIG. 8B

202002209600

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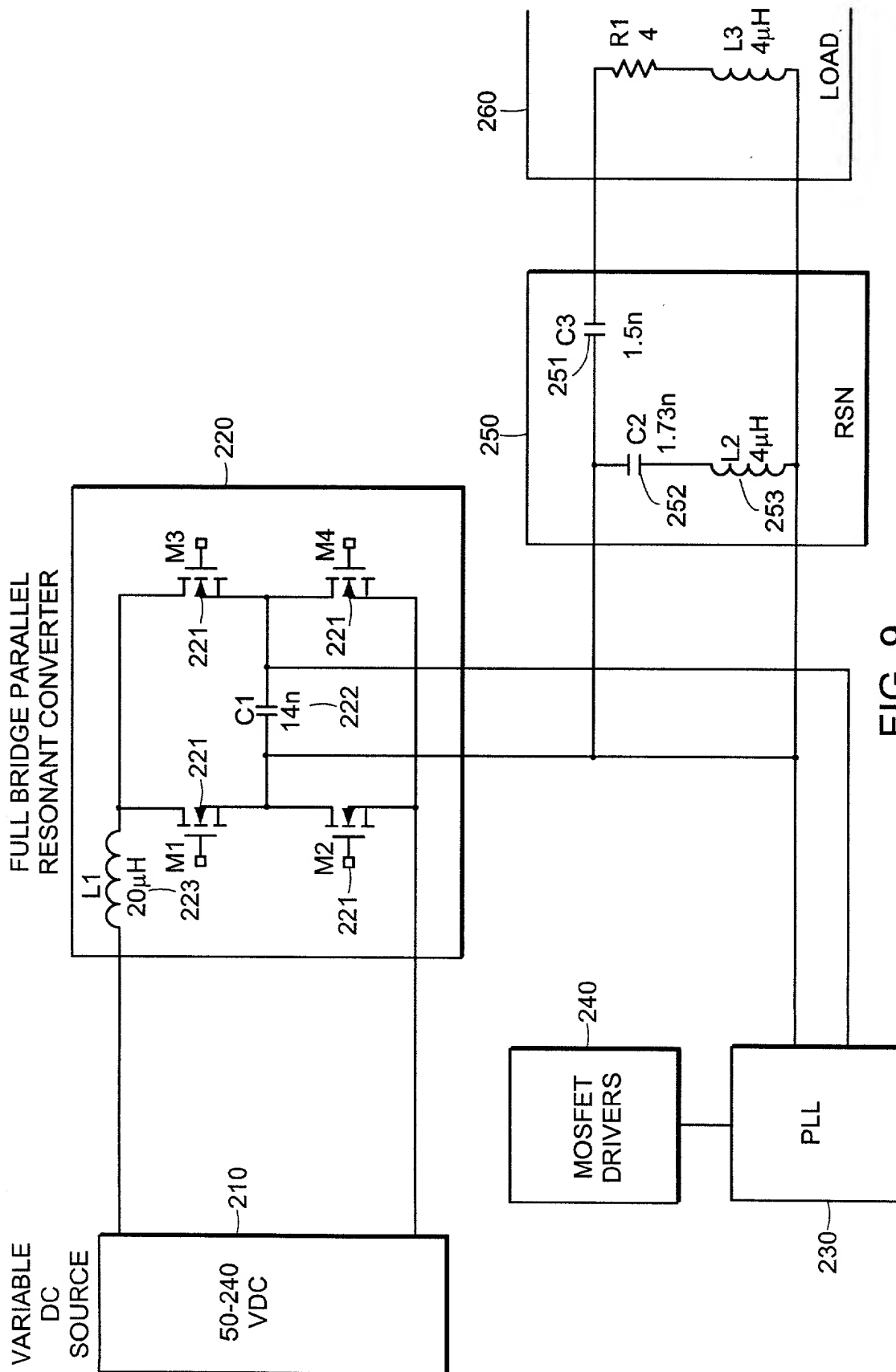


FIG. 9

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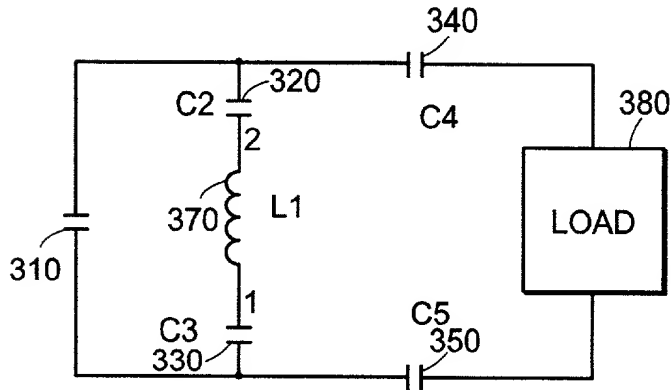


FIG. 10

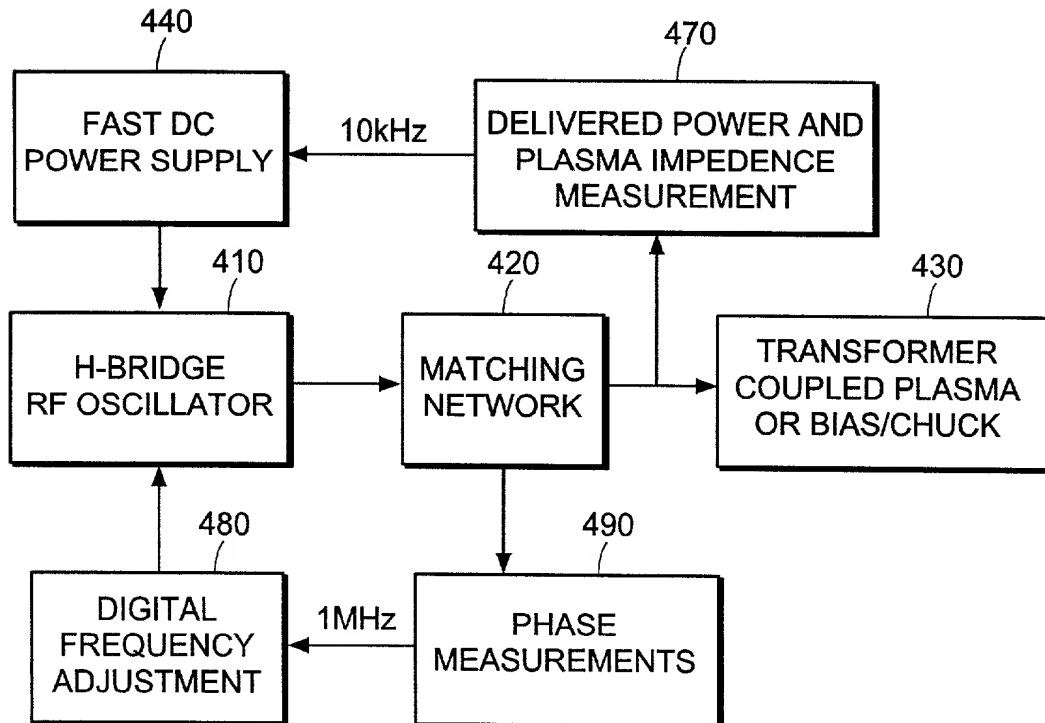


FIG. 11

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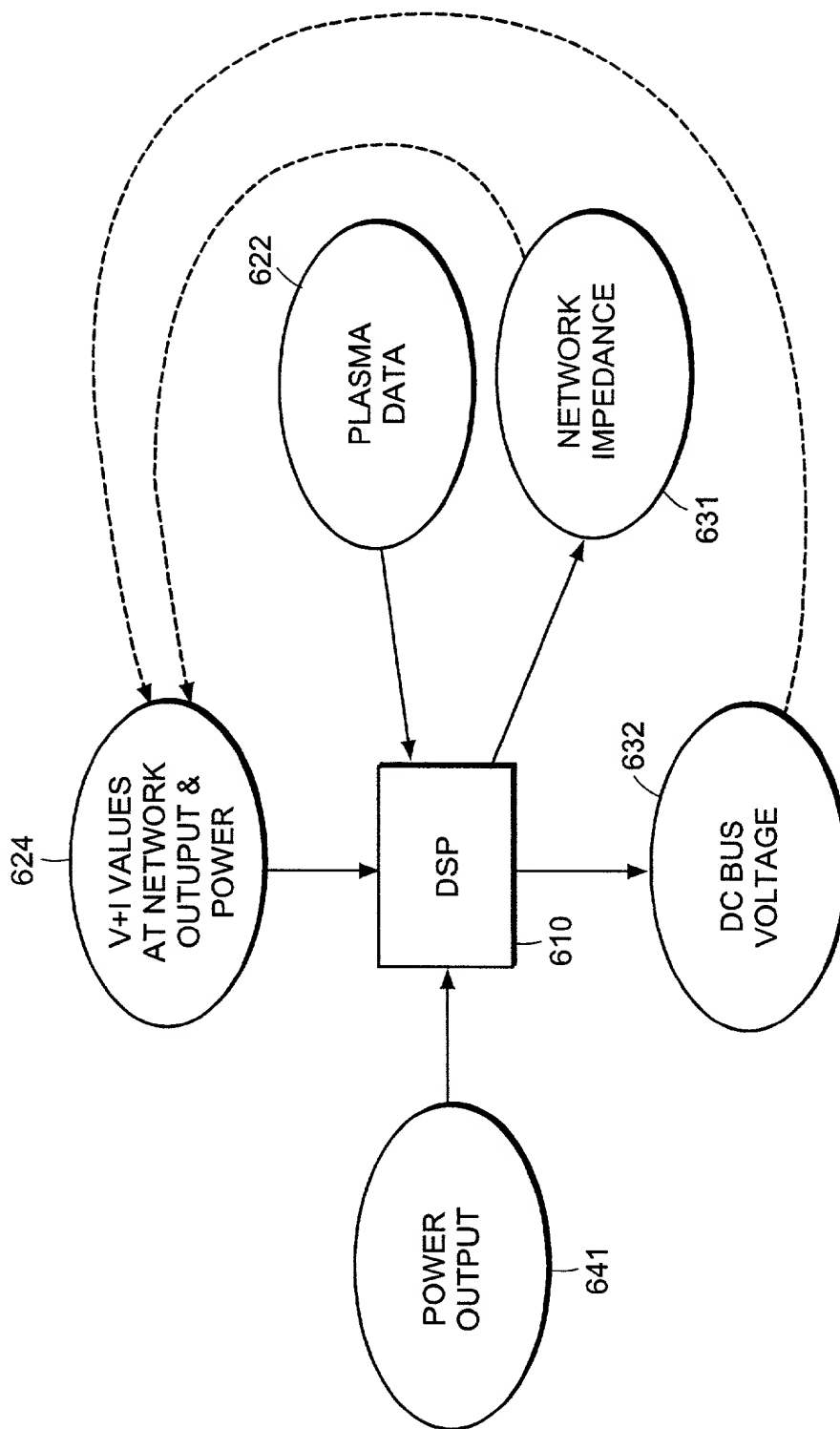


FIG. 12

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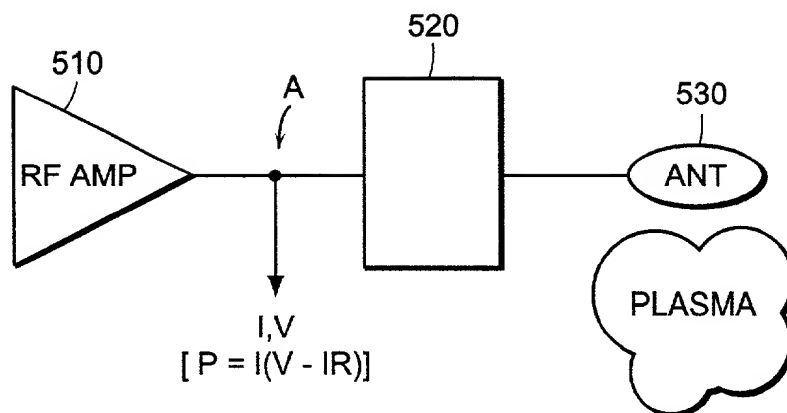


FIG. 13A

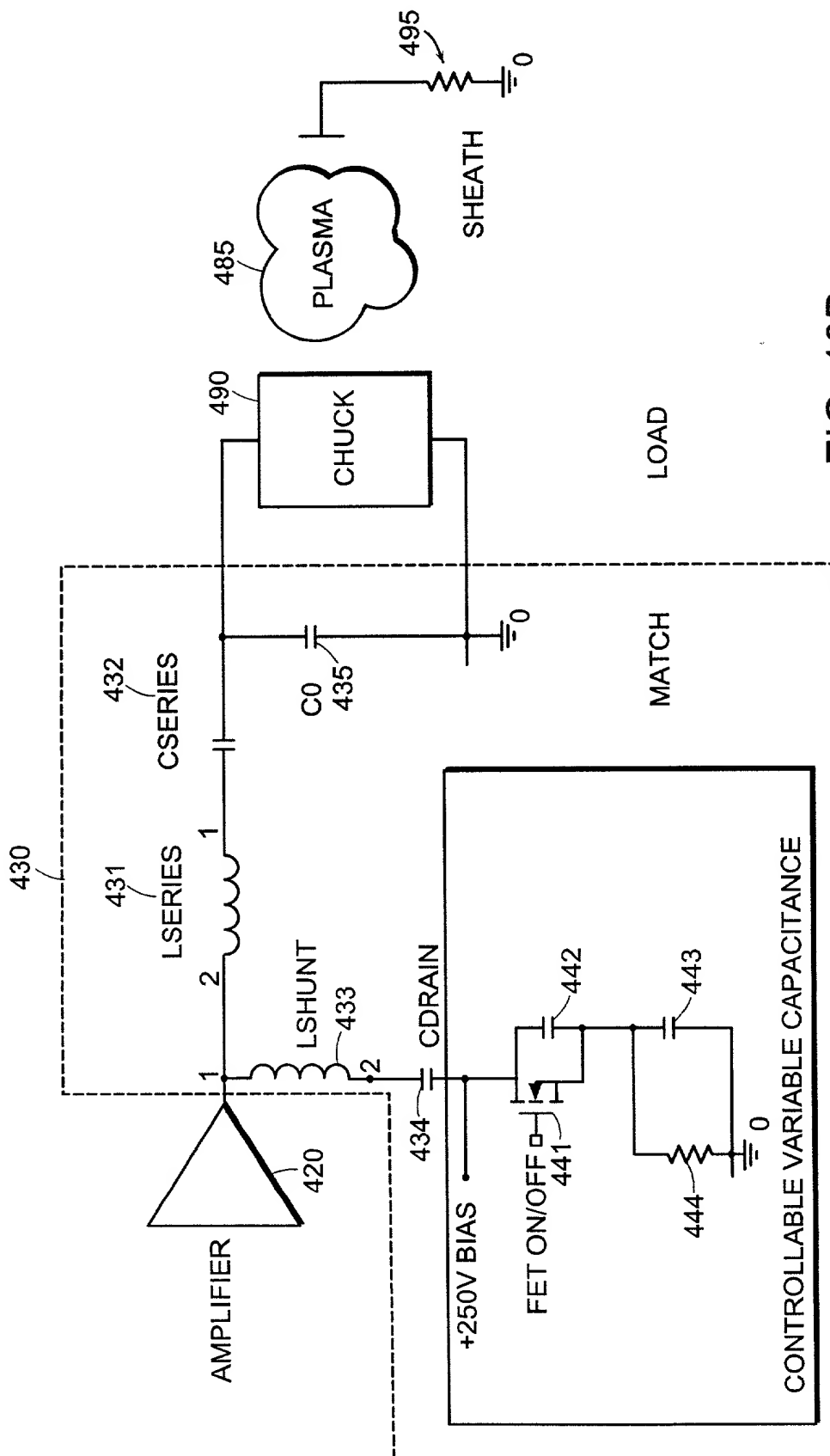


FIG. 13B

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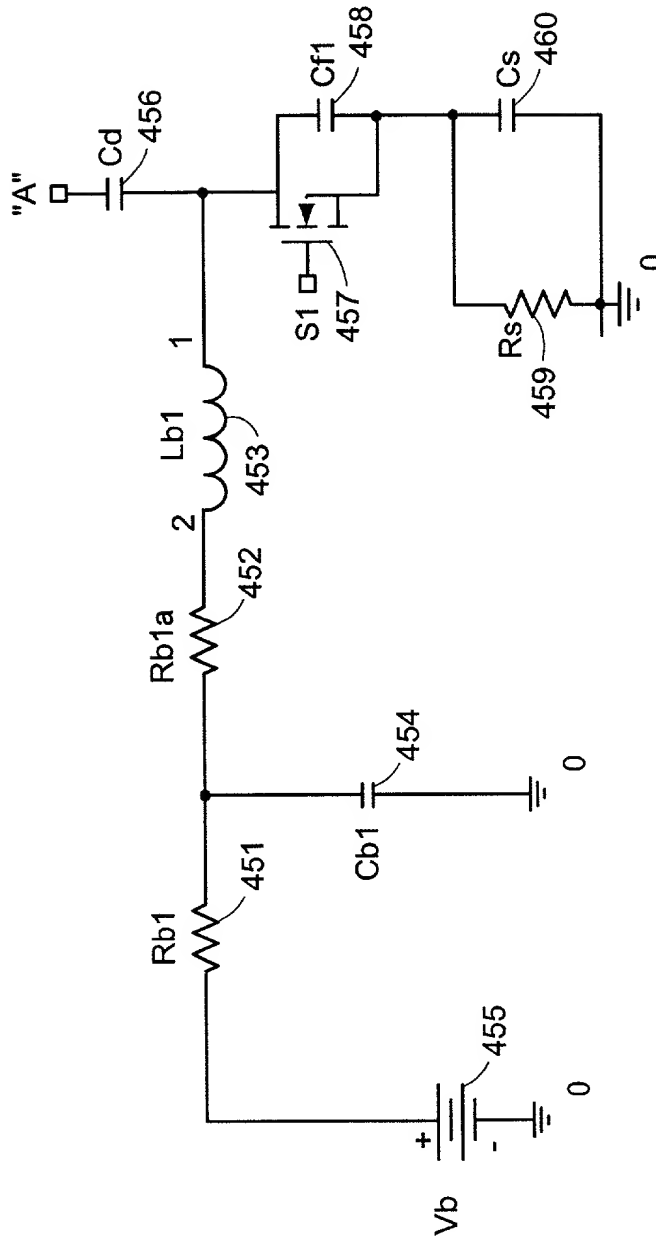


FIG. 14

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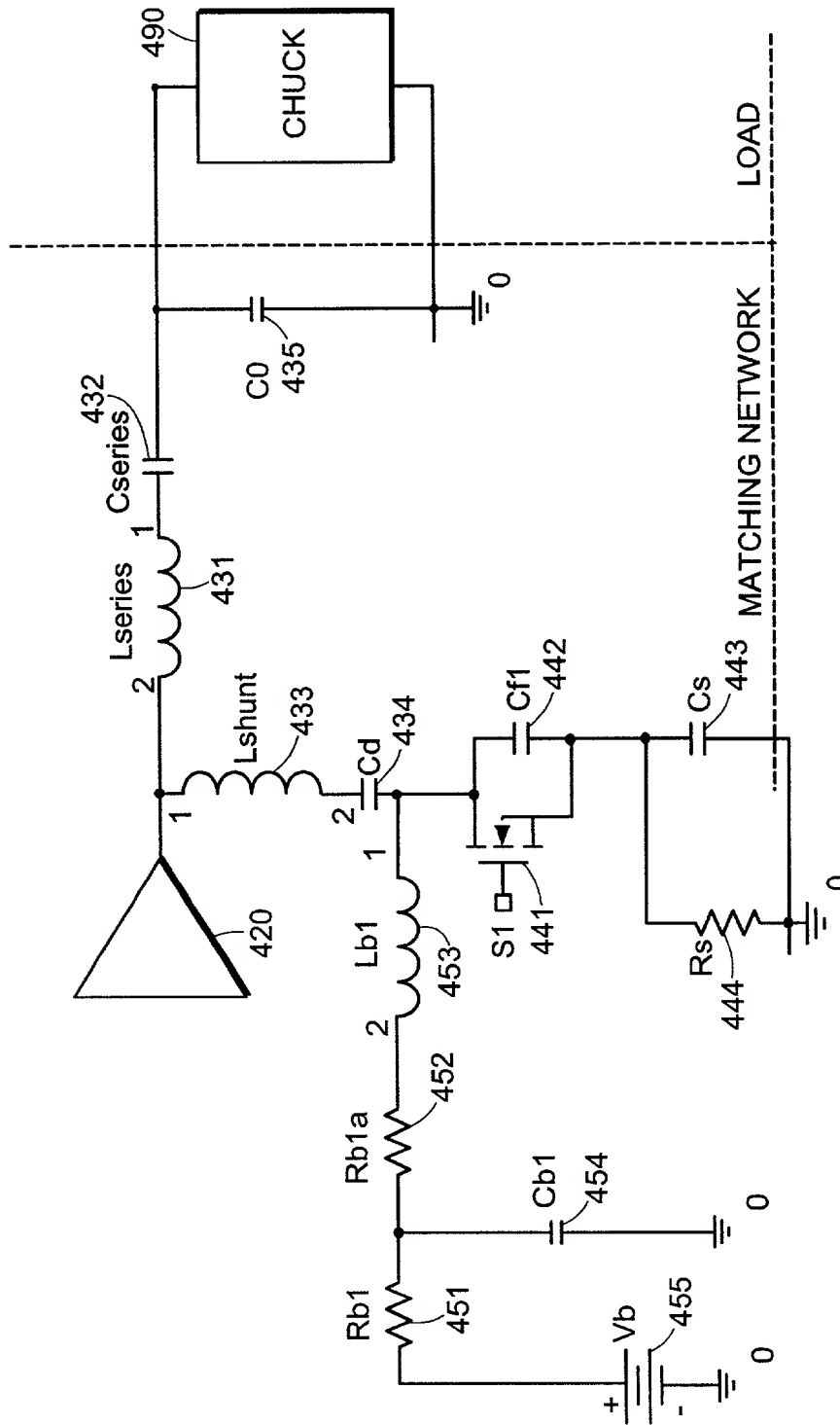
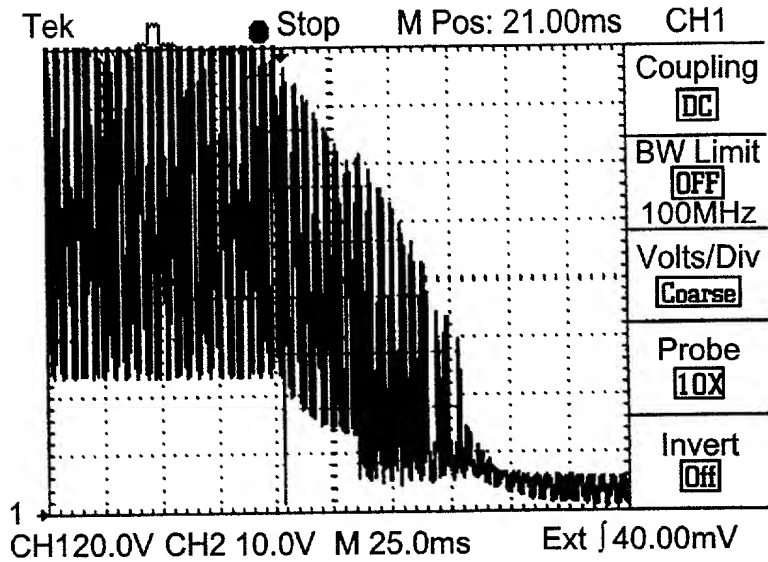


FIG. 15

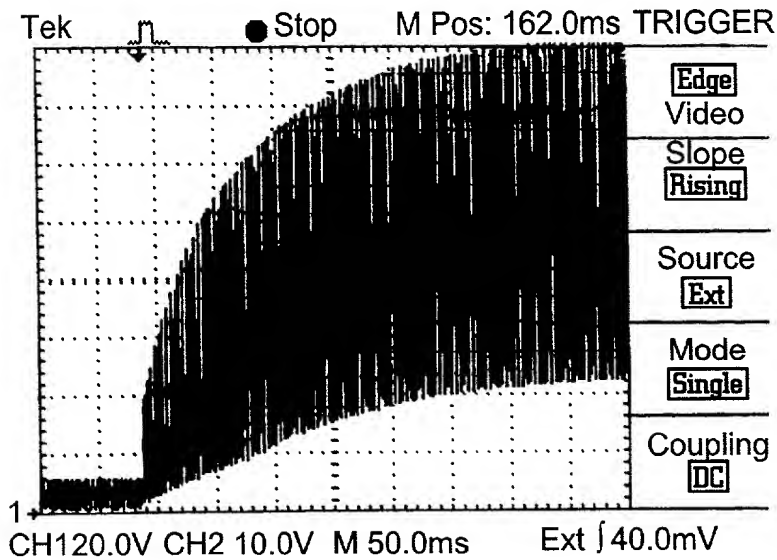
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25 ms/div

FET Turn-on

FIG. 16A



50 ms/div

FET Turn-off

FIG. 16B

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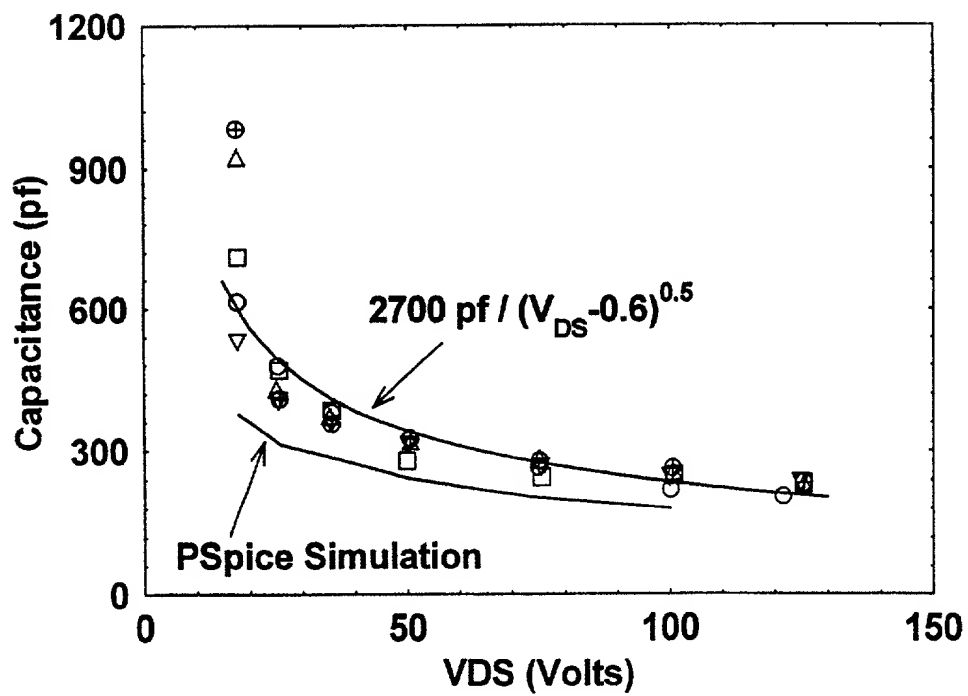


FIG. 17

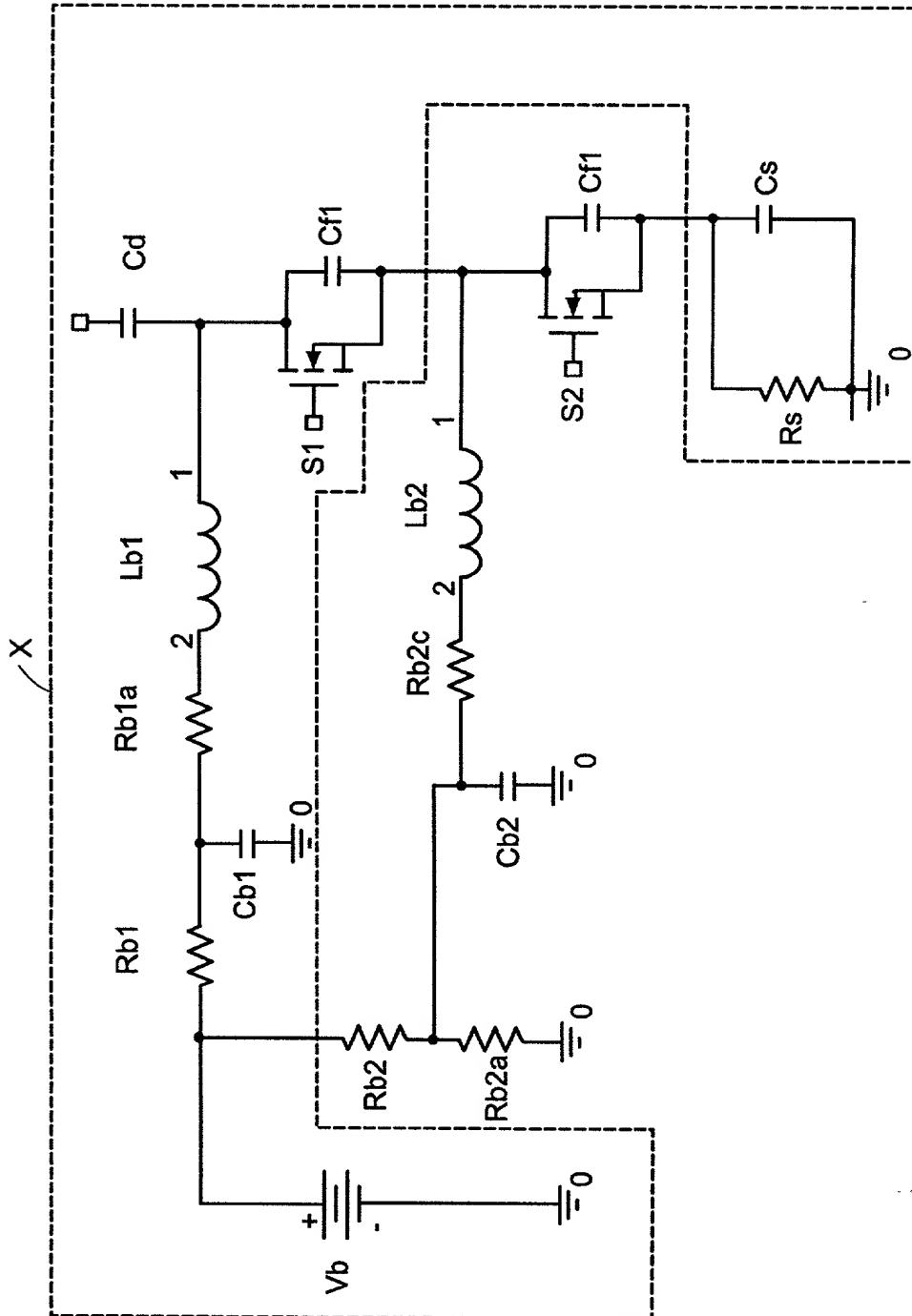


FIG. 18